UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/553,044	10/13/2005	Torayuki Tsukada	10921.361USWO	1677

52835 7590 04/16/2007

HAMRE, SCHUMANN, MUELLER & LARSON, P.C.
P.O. BOX 2902
MINNEAPOLIS, MN 55402-0902

EXAMINER	
COLEMAN, WILLIAM D	
ART UNIT	PAPER NUMBER
2823	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/553,044	TSUKADA, TORAYUKI	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

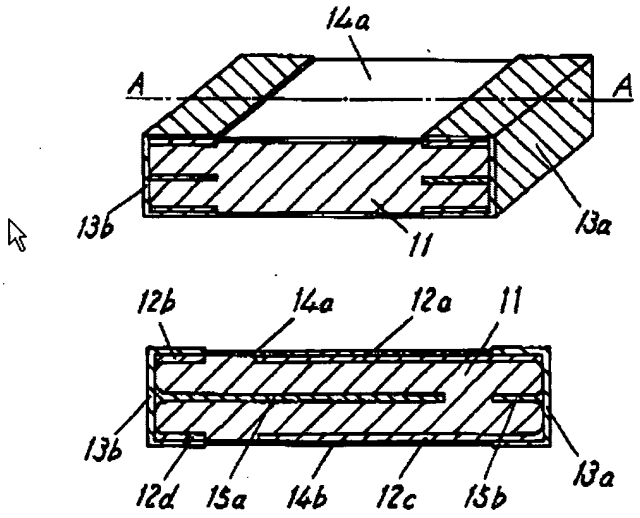
Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kojima et al., U.S. Patent 6,348,852 B1.

3. Kojima discloses a chip resistor as claimed. See **FIGS. 1(a)-11(b)**, where Kojima teaches the following limitations.



4. Pertaining to claim 1, Kojima discloses a chip resistor comprising:

a resistor element including a first surface and a second surface opposite to the first surface;

at least two main electrodes 12a, 12b spaced from each other and provided on the first surface; and

at least two auxiliary electrodes **12c** and **12d** spaced from each other and provided on the second surface, the auxiliary electrodes facing the main electrodes via the resistor element **11**;

wherein the main electrodes and the auxiliary electrodes are made of the same material (i.e., copper foil, see column 3, lines 43-44).

5. Pertaining to claim 2, Kojima teaches the chip resistor according to claim 1, wherein a spacing distance between the auxiliary electrodes is no smaller than a spacing distance between the main electrodes (please note that the gap between electrodes **12a** and **12b** is the same distance between electrodes **12d** and **12c**).

6. Pertaining to claim 3, Kojima teaches the chip resistor according to claim 1, further comprising a first insulating layer **14a** and a second insulating layer **14b** formed on the resistor element, wherein the first insulating layer covers an area between the main electrodes on the first surface of the resistor element, and the second insulating layer covers an area between the auxiliary electrodes on the second surface of the resistor element.

7. Pertaining to claim 4, Kojima teaches the chip resistor according to claim 3, wherein a thickness of the first insulating layer is no greater than a thickness of the main electrodes.

8. Pertaining to claim 5, Kojima teaches the chip resistor according to claim 1, further comprising at least two solder layers **13a, 13b** formed on the resistor element, wherein the resistor element includes a pair of end surfaces spaced from each other, each of the end surfaces being covered by a corresponding one of the two solder layers.

9. Pertaining to claim 6, Kojima teaches the chip resistor according to claim 5, the solder layers cover the main electrodes and the auxiliary electrodes in addition to the end surfaces of the resistor element.

10. Pertaining to claim 8, Kojima teaches the method of making a chip resistor, the method comprising the steps of:

preparing a resistor material **11** including a first surface and a second surface opposite the first surface;

forming a pattern of the first conductive layer on the first surface;

forming a pattern of second conductive layer on the second surface; and

dividing the resistor material into a plurality of resistor elements;

wherein the first conductive layer and the second conductive layer are made of the same material.

11. Pertaining to claim 9, Kojima teaches the method of making chip resistor according to claim 8, wherein the dividing of the resistor material is performed in a manner such that a

resulting chip resistor comprises a main electrode made of a part of the first conductive layer and also comprises an auxiliary electrodes made of a part of the second conductive layer.

12. Pertaining to claim 10, Kojima teaches the method of making chip resistor according to claim 8, further comprising an additional step, performed before the pattern forming of the first conductive layer, for forming a patter of the first insulating layer on the first surface of the resistor material and also a pattern of a second insulating layer on the second surface of the resistor material, wherein the first conductive layer and the second conductive layer are formed on areas of the resistor material where the first and the second insulating layers are not formed.

13. Pertaining to claim 11, Kojima teaches the method of making chip resistor according to claim 10, wherein the pattern forming of the insulating layer is formed by thick-film printing.

14. Pertaining to claim 12, Kojima teaches the method of making chip resistor according to claim 10, wherein the first conductive layer and the second conductive layer are made by metal plating (please note that it is well known to form copper foil by metal plating).

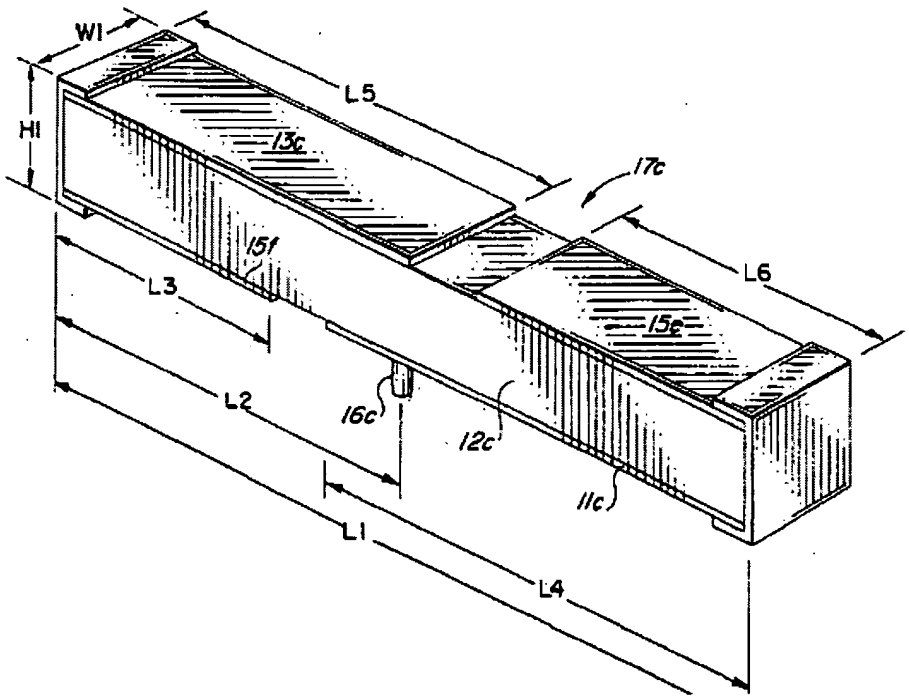
Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kojima et al, U.S. Patent 6,348,852 B1 in view of Ko et al, U.S. Patent 5,781,158.

Kojima discloses a semiconductor device and process substantially as claimed. However, Kojima fails for form a third insulating layer wherein the side surface is covered by a third insulating layer.



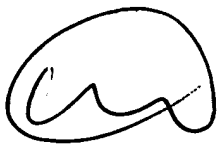
The image above is attributed to Ko, where surfaces 12a, 12b and 12c are insulating layers. In view of Ko, it would have been obvious to one of ordinary skill in the art to incorporate the chip resistor fabrication methods of Ko into the Kojima semiconductor process because the stacked dielectric located on the ground plate will prevent leaking current (see column 11, lines 1-7).

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

18. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

19. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



W. David Coleman
Primary Examiner
Art Unit 2823

WDC